

PATENT ABSTRACTS OF JAPAN

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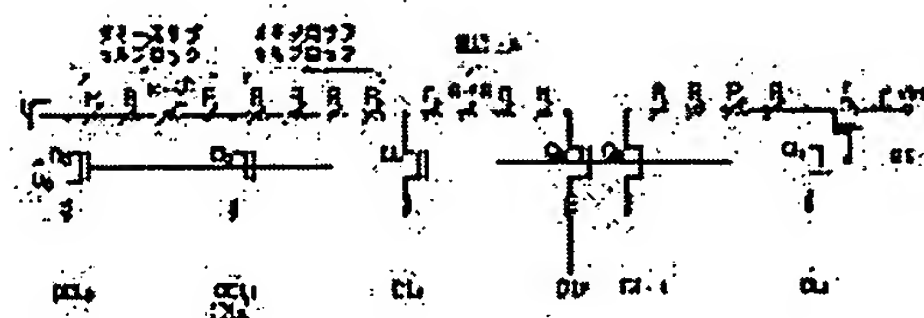
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(54) SEMICONDUCTOR MEMORY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce a voltage drop variation based on a resistance parasitic in transistors and wirings and enable stable and high speed operation even when a signal read from a cell is small by reading data from the nodes at both ends of a sub-cellblock formed by connecting in series the memory cells in the bit line direction.

SOLUTION: A magneto-resistive film consisting of a three-layer structure of ferro-magnetic layer, non-magnetic conductive layer and ferro-magnetic layer is connected to a bit line, data '1' is stored when the spins of the magnetic layers of the upper layer and lower layer are in the inverted direction (resistance of bit line is R) and data '0' is stored when these are in the same direction (resistance of bit line is $R - \Delta R$). A cell block is structured by connecting in series a plurality of sub-cellblocks consisting of series connection of four memory cells. In the case of the reading operation, a voltage is applied to V_{int} , V_s at both ends of the cell block to generate a current in the bit line and the data lines DDL_0 to DDL_n led from both ends of the selected sub-cellblock are connected to the sense amplifier of high impedance.



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